AMENDMENTS TO THE CLAIMS

Claim 1-5 (Canceled)

Claim 6 (Currently Amended) An apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

assigning a first register class to at least one symbolic register in at least one instruction;

~~determining and~~ assigning a second register class to the at least one symbolic register through conjunctive forward dataflow analysis;

reducing register class fixups for the assignment of the second register class; and

renaming the at least one symbolic register.

Claim 7 (Original) The apparatus of claim 6, said assigning the first register class instruction is an initial assignment.

Claim 8 (Currently Amended) The apparatus of claim 6, said ~~determining and~~ assigning the second register class further including instructions which, when executed by a machine, cause the machine to perform operations including:

marking a register class assignment map at a block entry;

marking a register class assignment map at a block exit;

determining a register class assignment map at an entry of a instruction; and

determining a register class assignment map at an exit of a instruction.

Claim 9 (Original) The apparatus of claim 6, said reducing register class fixups further including instructions which, when executed by a machine, cause the machine to perform operations including:

hoisting register class fixups;

sinking register class fixups; and

removing unnecessary register class fixups.

Claim 10 (Original) The apparatus of claim 9, said removing unnecessary register class fixups further including instructions which, when executed by a machine, cause the machine to perform operations including removing dead code.

Claim 11 (Currently Amended) A system comprising:

a processor having at least one register; and

a compiler coupled to the processor executing in a host device that inputs a source program having a plurality of operation blocks,

wherein the compiler assigns a first register class in at least one instruction to the at least one symbolic register, ~~determines~~ and assigns a second register class through conjunctive forward dataflow analysis to the at least one symbolic register, reduces register class fixups for the assignment of the second register class, and renames the at least one symbolic register.

Claim 12 (Original) The system of claim 11, wherein the first register class assigned is an initially assigned register class.

Claim 13 (Currently Amended) The system of claim 11, wherein the second register class ~~determined and~~ assigned includes:

marking a register class assignment map at a block entry;

marking a register class assignment map at a block exit;

determining a register class assignment map at an entry of a instruction; and

determining a register class assignment map at an exit of a instruction.

Claim 14 (Original) The system of claim 11, said reduction of register class fixups includes:

hoisting register class fixups;

sinking register class fixups; and

removing unnecessary register class fixups.

Claim 15 (Original) The system of claim 14, said removing unnecessary register class fixups includes removing dead code.

Claim 16 (Currently Amended) A computer comprising:

at least one processor having at least one register coupled to a first memory and a second memory;

at least one user input device coupled to the processor;

a monitor coupled to the processor, and

a compiler executing in the processor that inputs a source program having a plurality of operation blocks,

wherein the compiler assigns a first register class in at least one instruction to the at least one register, ~~determines and~~ assigns a second register class through conjunctive forward dataflow analysis to the at least one register, reduces register class fixups for the assignment of the second register class, and renames the at least one register.

Claim 17 (Original) The computer of claim 16, wherein the first register class assigned is an initially assigned register class.

Claim 18 (Currently Amended) The computer of claim 16, wherein the second register class ~~determined and~~ assigned includes:

marking a register class assignment map at a block entry;

marking a register class assignment map at a block exit;

determining a register class assignment map at an entry of a instruction; and

determining a register class assignment map at an exit of a instruction.

Claim 19 (Original) The computer of claim 16, said reduction of register class fixups includes:

hoisting register class fixups;

sinking register class fixups; and

removing unnecessary register class fixups.

Claim 20 (Original) The system of claim 19, said removing unnecessary register class fixups includes removing dead code.